

**WHAT IS CLAIMED IS:**

1. A circuit for controlling a vector scatter instruction wherein an area-specified vector scatter instruction specifying scattered areas is provided as an instruction set, comprising:

means for detecting if an address to be accessed by the area-

5 means for holding the memory access instruction that follows the vector scatter instruction if the addresses overlap; and

means for holding the memory access instruction that follows the vector scatter instruction if the addresses overlap.

2. The circuit as defined in claim 1 wherein the memory access instruction that follows the vector scatter instruction is held until cache invalidation is finished.

3. A vector architecture information processing equipment comprising:

a vector scatter address coincidence detection unit including:

a plurality of registers for storing an area start address and an

5 area end address of an area-specified vector scatter instruction in which the area start address and the area end address are specified; and

a circuit for checking if an address to be accessed by a memory access instruction following the area-specified vector scatter instruction is within a scatter area defined by the area start address and the area end address specified by the area-specified vector scatter instruction to outputs an address coincidence signal if the address to be accessed by the following memory access instruction is within the scatter area,

wherein an instruction issue control unit comprises a hold control circuit for holding said following memory access instruction  
15 upon receipt of an address coincidence signal emitted from said vector scatter address coincidence detection unit.

4. A vector architecture information processing equipment comprising:

an instruction issue control unit decoding an instruction data to direct an instruction operation;

5 a cache control unit receiving an address from said instruction issue control unit to control a cache;

a vector unit, on receipt of an execution directive when a vector instruction is issued from said instruction issue control unit sending write vector data to a memory and sending a cache invalidation address, if the vector instruction is an area-specified vector scatter instruction specifying an area start address and an area end address of a scatter area;

a cache invalidation control unit receiving the cache invalidation address from said vector unit to invalidate the cache; and

15 a vector scatter address conflict detection unit, on receipt of the area start address and the area end address of the area-specified vector scatter instruction from a register block accessed by said instruction issue control unit when the area-specified vector scatter instruction is issued from said instruction issue control unit,

20 detecting if an area specified by the area start address and the area end address overlaps with an address area to be accessed by a

memory access instruction following the area-specified vector scatter instruction to activate an address coincidence signal for sending said signal to said instruction issue control unit if an address overlap is  
25 detected,

wherein said instruction issue control unit comprises a hold control circuit that holds the following memory access instruction in response to the activated address conflict signal from said vector scatter address conflict detector.

5. The vector architecture information processing equipment as defined in claim 4 wherein said hold control circuit does not hold the following memory access instruction if the address coincidence signal from said vector scatter address coincidence detection unit is inactive.

6. The vector architecture information processing equipment as defined in claim 4 wherein said hold control circuit holds the following memory access instruction until a cache invalidation end notification is received from said cache invalidation control unit.

7. The vector architecture information processing equipment as defined in claim 4 wherein said vector scatter address coincidence detection unit comprises:

a first comparator that compares the address to be accessed by

5 the following memory access instruction with the area start address specified by the area-specified vector scatter instruction and, if the address to be accessed by the following memory access instruction is equal to or larger than the area start address, outputs an active signal;

a second comparator that compares the address to be accessed

10 by the following memory access instruction with the area end address specified by the area-specified vector scatter instruction and, if the address to be accessed by the following memory access instruction is equal to or smaller than the area end address, outputs an active signal; and

15 a logical circuit that activates the address conflict signal and outputs the signal if both output signals from said first comparator and the output from said second comparator are active.

8. The vector architecture information processing equipment as defined in claim 4 wherein an operand of the area-specified vector scatter instruction comprises a predetermined field for specifying two registers in which the scatter area start address and the scatter area end

5 address are respectively specified, said two registers being included in said register block.

9. The vector architecture information processing equipment as defined in claim 4 wherein, when at least one instruction follows said following memory access instruction, said hold control circuit also holds said one instruction in each corresponding stage in response to the

5 activated address coincidence signal from said vector scatter address coincidence detection unit.

10. The vector architecture information processing equipment as defined in claim 4 wherein an operand of the area-specified vector scatter (VSC) instruction comprises X, Y, and Z fields for specifying

10 respectively X register, Y register, and R<sub>n</sub> register of two registers R<sub>n</sub> and R<sub>n+1</sub> in which the scatter area start address and the scatter area end

address are respectively specified, said two registers being included in said register block,

    said instruction issue control unit comprising:

15       an instruction cache for storing instruction data read from a memory;

    a first stage register for storing an operation code and operand fields of an instruction sent from said instruction cache;

20       an increment circuit for incrementing a register number for specifying a two consecutive registers R<sub>n</sub> and R<sub>n+1</sub> in the register block, in which the scatter area start address and the scatter area end address are respectively specified;

    a register update control unit for controlling update of registers in the register block;

25       a second stage register for storing operation code, X field and Y field of the operand read moved the first stage register;

    a third stage register to which information in the second stage register is moved for outputting a vector instruction issue directive information to the vector unit wherein in case of the VSC instruction, 30 the output from the third stage register indicates a vector register number, said vector register number being supplied to the vector unit; and

    a third stage address register for storing an address in case of scalar load (LDS) instruction for use in accessing the cache;

35       Y data and Z data registers for storing operand data read from the register located in the second stage;

said address coincidence detection unit comprises:

a VSC start address latch and a VSC end address latch located in said third stage, in which a VSC start address and a VSC end address  
40 read via the Y and Z data registers in the second stage are stored, respectively, wherein the VSC start address latch and the VSC end address latch on receipt of a hold signal supplied from said hold control circuit to hold the VSC start address and the VSC end address;

a VSC start address latch and the VSC end address latch  
45 located in a fourth stage wherein data held in the VSC start address latch and the VSC end address latch, strobed by a VSC issue signal from the hold control unit, is set and retained until a next area-specified VSC instruction is issued,

a first comparator that receives outputs of said third stage  
50 address register and said fourth stage VSC start address latch;

a second comparator that receives outputs of said third stage address register and said fourth stage VSC end address latch;

a logic circuit receiving comparison results of said first and second comparators to output an address coincidence signal to said hold  
55 control unit, said hold control unit, upon receipt of the address coincidence signal outputting a hold signals respectively to said first stage register, said second stage register, said third stage register, and said third stage address register,

wherein in case that an address to be accessed by a LDS  
60 instruction that is issued immediately following the area-specified VSC instruction does not overlap with the scatter area of the VSC instruction,

the address coincidence signal is inactivated and sent to said hold control unit, said hold control unit not activating the hold signal, whereas in case that an address to be accessed by the following LDS  
65 instruction overlaps with the scatter area of the VSC instruction, the address coincidence signal is activated and sent to said hold control unit, said hold control unit, by activating the hold signal to said third stage VSC start address latch and a VSC end address latch, said hold signal being kept in an activated state until a cache invalidation end signal  
70 output from the cache invalidation control unit indicates that the cache invalidation processing is completed, while the following LDS instruction being held in the third stage of the instruction issue control unit.